METHOD FOR ACCESSING A SINGLE PORT MEMORY

DESCRIPTION

CROSS-REFERENCE TO RELATED APPLICATION

[Para 1] This application claims the priority benefit of Taiwan application serial no. 93117282, filed June 16, 2004.

BACKGROUND OF THE INVENTION

[Para 2] Field of the Invention

[Para 3] The present invention relates to a method for accessing a single port memory.

[Para 4] Description of the Related Art

[Para 5] In order to rearrange and provide the received pixel data based on the requirement of different operation mode, a line buffer is commonly used in the LCD timing controller to cache the line pixel data, such that the line pixel data can be accurately transmitted by the timing controller. Wherein, in order to support the read and write operations simultaneously, a dual port memory is commonly used as the line buffer. However, the dual port memory occupies large space inside the integrated circuit (IC), thus it is hard to reduce the product cost and size.

SUMMARY OF THE INVENTION

[Para 6] Therefore, the object of the present invention is to provide a method for accessing a single port memory. In this method, a single port

memory is used as the line buffer in a display control circuitry or in a liquid crystal display system to fulfill the requirement of simultaneously reading and writing the line buffer.

[Para 7] In order to achieve the above and other objects, the present invention provides a method for accessing a single port memory, which can safely and simultaneously access the line data operated in a normal mode. The method comprises the following steps: dividing a single port line buffer into N memory blocks, wherein N is an integer; receiving the line data, and sequentially writing the received line data into the divided N memory blocks; after writing more than N/2+1 memory blocks, reading out the line data from the memory blocks based on the requirement of the normal mode operation; and sequentially writing a next line data into the memory block where the stored line data has been completely read out.

[Para 8] Wherein, the single port line buffer may be divided into 8 memory blocks.

[Para 9] Alternatively, the reading of the line data from the memory blocks may start after the writing of N/2+2 memory blocks is completed based on the requirement of the normal mode operation.

[Para 10] The present invention further provides a method for accessing a single port memory, which can safely and simultaneously access the line data which is operated in PLM mode. The method comprises the following steps: dividing a single port line buffer into N memory blocks, wherein N is an integer; receiving the line data, and writing the even data and odd data of the line data into the divided N memory blocks with a sequence of 1^{st} memory block and $(N/2+1)^{th}$ memory block, 2^{nd} memory block and $(N/2+2)^{th}$ memory block, ..., etc, respectively; after writing more than N/2+1 memory blocks, reading out the line data from the memory blocks based on the requirement of the PLM mode operation; and sequentially writing the even data and odd data of next line data into the memory block where the stored line data has been completely read out, respectively.

[Para 11] Wherein, the single port line buffer may be divided into 8 memory blocks.

[Para 12] Alternatively, the reading of the line data from the memory blocks may start after the writing of N/2+2 memory blocks is completed based on the requirement of the PLM mode operation.

[Para 13] In summary, in the method for accessing the single port memory in the present invention, the single port line buffer is divided into N memory blocks, and different memory blocks in the line buffer are sequentially read out or written into based on the requirement of the normal mode or PLM mode operation. Therefore, the single port memory can be used in the display control circuitry or in the liquid crystal display system as the line buffer, such that the requirement of simultaneously reading and writing the line buffer is achieved.

BRIEF DESCRIPTION OF THE DRAWINGS

[Para 14] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention, and together with the description, serve to explain the principles of the invention.

[Para 15] FIG. 1 schematically shows a timing diagram for illustrating a line buffer access operation under a normal mode.

[Para 16] FIG. 2 schematically shows a timing diagram for illustrating a line buffer writing completion operation under a normal mode.

[Para 17] FIG. 3 schematically shows a timing diagram for illustrating a line buffer write/read operation under a normal mode.

[Para 18] FIG. 4 schematically shows a timing diagram for illustrating a line buffer access operation under a PLM mode.

[Para 19] FIG. 5 schematically shows a timing diagram for illustrating a line buffer writing completion operation under a PLM mode.

[Para 20] FIG. 6 schematically shows a timing diagram for illustrating a line buffer write/read operation under a PLM mode.

DESCRIPTION OF EMBODIMENTS

[Para 21] For a clear explanation and better understanding of the method for accessing the single port memory in the present invention, a display control circuitry supporting UXGA is exemplified hereinafter. Each UXGA line has 1600 pixels, thus the line buffer in the display control circuitry can store a line data of up to 1600 pixels, wherein the line buffer is a single port memory. In addition, assuming that all memory blocks in the line buffer can be accessed with the same speed, the example that the line buffer is divided into 8 memory blocks, wherein each memory block stores a line data of 200 pixels, is used hereinafter to describe how to safely access different memory block in the line buffer in the right sequence. It will be apparent to those skilled in the art that the line buffer may be divided into different number of memory blocks based on different requirement.

[Para 22] FIG.1 schematically shows a timing diagram for illustrating a line buffer access operation under a normal mode. In FIG. 1, R0, G0, B0 represents the Red (R), Green (G), Blue (B) color data of the pixel 0 in the line, respectively; R1, G1, B1 represents the Red (R), Green (G), Blue (B) color data of the pixel 1 in the line, respectively; ..., etc.

[Para 23] As shown in FIG. 1, under the normal mode operation, when a writing signal WREN is enabled, the line data R0, G0, B0, R1, G1, B1, ..., R1599, G1599, B1599, are sequentially written into the line buffer. Of course, the example shown above refers to writing a data of two pixels into the line buffer simultaneously. Then, when a reading signal RDEN is enabled, a line data of each pixel from pixels 0 ~ 799 and pixels 800 ~ 1599 is sequentially read. Therefore, after the line data is received by the display control circuitry, the display control circuitry first sequentially writes the received line data into the divided 8 memory blocks, and the process of writing completion is shown in

FIG. 2, wherein the numbers are used to represent the pixel id of the stored line data. During the reading operation, in order to fulfill the requirement of sequentially reading the line data of each pixel from pixels 0 ~ 799 and pixels 800 ~ 1599, each pixel data from block 1 and block 5 has to be sequentially read first, and each pixel data from block 2 and block 6 has to be sequentially read after the reading of the memory blocks mentioned above is completed, ..., etc.

[Para 24] Since the line buffer used here is a single port memory, which cannot perform the read and write operations on the same memory block simultaneously, the read operation is only started after the writing of the 5th memory block is completed. In the present embodiment, the reading of the line data from the memory block is started after the writing of the 6th memory block is completed based on the requirement of the normal mode operation. After the reading operation is started, since the next line data can overwrite the memory block only after the memory block has been completely read out, the next line data is then sequentially written into the memory block where the stored line data has been completely read out, wherein the sequence of reading and writing of the first several lines is shown in FIG. 3, and others follow the same order.

[Para 25] As shown in FIG. 3, the numbers '1' to '8' on X-axis are the memory block id, and the numbers '1' to '24' on Y-axis are the time section id of the time required for reading and writing one memory block. According to the access sequence mentioned above, a full read and write cycle is completed after running 24 time sections, thus the time section id is reset to '1' after number '24'. Wherein, Wxx and Rxx represent the data block of the writing and reading id xx, respectively, and F1 ~ F4 and B1 ~ B4 represent the line data block of the pixels 0 ~ 199, 200 ~ 399, 400 ~ 599, 600 ~ 799, and pixels 800 ~ 999, 1000 ~ 1199, 1200 ~ 1399, 1400 ~ 1599, respectively. As shown in FIG. 3, since in the reading method of the normal mode operation, each data of one memory block, for example, the data block where F1 is stored and the data block where B1 is stored, are read simultaneously by turns. Therefore, the reading operation is performed during the 7th and 8th time sections, and

the line data F1 and F2 of next line are sequentially written into the 1st and 5th memory blocks where the stored line data has been completely read out during the 9th and 10th time sections.

[Para 26] Therefore, with the method for accessing the single port memory in the present invention, different memory blocks in the single port line buffer are accessed by turns based on the requirement of the normal mode operation. Accordingly, the single port memory can be used as the line buffer in the liquid crystal display panel, so as to fulfill the requirement of simultaneously reading and writing the line buffer without any clashing.

[Para 27] FIG. 4 schematically shows a timing diagram for illustrating a line buffer access operation under a PLM mode. As shown in FIG. 4, R0, G0, B0 represents the Red (R), Green (G), Blue (B) color data of the pixel 0 in the line, respectively; R1, G1, B1 represents the Red (R), Green (G), Blue (B) color data of the pixel 1 in the line, respectively; ..., etc.

[Para 28] As shown in FIG. 4, under the PLM mode operation, when a writing signal WREN is enabled, the line data R0, B0, G1, G0, R1, B1, ..., G1598, R1599, B1599, are sequentially written into the line buffer. Of course, in order to fulfill the requirement of the PLM mode operation, the example shown above refers to writing an even number of even data R0, B0, G1, which are arranged in a sequence starting from 0 among R0, G0, B0, R1, G1, B1, and the odd number of odd data G0, R1, B1, which are arranged in a sequence starting from 0 among R0, G0, B0, R1, G1, B1 into the memory blocks, respectively. The top and bottom rows of the written data shown in FIG. 4 are sequentially written into the divided 8 memory blocks in a sequence of 1st memory block and 5th memory block, 2nd memory block and 6th memory block, ..., etc, respectively. Afterwards, when the reading signal RDEN is enabled, the line data stored in the memory block 1, memory block 2, memory block 3, are sequentially read out. Therefore, after the line data is received by the display control circuitry, the display control circuitry first writes the even data and odd data of the line data into the blocks 1 ~ 4 and blocks 5 ~ 8 of the divided 8 memory blocks in a sequence shown in FIG. 4, respectively. The process of writing completion is shown in FIG. 5, wherein the numbers represent the

sequence number of the even data and odd data. During the reading operation, the line data in memory block 1, memory block 2, memory block 3 are sequentially read out, such that the even data is read first, and the odd data is read later, so as to fulfill the requirement of the PLM mode operation shown in FIG. 4.

[Para 29] Of course, since the line buffer used here is a single port memory, which cannot perform the read and write operations on the same memory block simultaneously, the read operation is only started after the writing of 5 memory blocks is completed. In the present embodiment, the reading of the line data from the memory block is started after the writing of 6 memory blocks is completed based on the requirement of the PLM mode operation. After the reading operation is started, since the next line data can overwrite the memory block only after the memory block has been completely read out, the even data and odd data of the next line data are then sequentially written into the memory block where the stored line data has been completely read out, wherein the sequence of reading and writing of the first several lines is shown in FIG. 6, and others follow the same order.

[Para 30] As shown in FIG. 6, the numbers '1' to '8' on X-axis are the memory block id, and the numbers '1' to '24' on Y-axis are the time section id of the time required for reading and writing one memory block. In the above description, a full read and write cycle is completed after running 24 time sections, thus the time section id is reset to '1' after number '24'. Wherein, Wxx and Rxx represent the data block of the writing and reading id xx, respectively, and E1 ~ E4 and O1 ~ O4 represent the data block of the even data and odd data, respectively. As shown in FIG. 6, since in the writing method of the PLM mode operation, each data of one memory block, for example, the data block where the even data E1 is stored and the data block where the odd data O1 is stored, are written into the memory block, respectively. Therefore, the writing operation is performed during the 1st and 2nd time sections, and the line data E1 and O1 of the next line are sequentially written into the 1st and 2nd memory blocks where the stored line data has been completely read out during the 9th and 10th time sections.

[Para 31] Therefore, with the method for accessing the single port memory in the present invention, different memory blocks in the single port line buffer are accessed by turns based on the requirement of the PLM mode operation. Accordingly, the single port memory can be used as the line buffer in the display control circuitry or in the liquid crystal display system, so as to fulfill the requirement of simultaneously reading and writing the line buffer without any clashing.

[Para 32] Although the invention has been described with reference to a particular embodiment thereof, it will be apparent to one of the ordinary skill in the art that modifications to the described embodiment may be made without departing from the spirit of the invention. Accordingly, the scope of the invention will be defined by the attached claims not by the above detailed description.